HIGH PERFORMANCE MMIC 20 GHz LNA AND 44 GHz POWER AMPLIFIER USING PLANAR-DOPED InGaAs HEMTs

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ABSTRACT

GaAs-based InGaAs Psuedomorphic High Electron Mobility Transistors (HEMT) have demonstrated superior low-noise and high power capabilities at microwave and millimeter wave frequencies. This paper presents a pair of 3-stage amplifiers fabricated with the same process demonstrating excellent noise and power performance. A K-Band fully monolithic LNA has demonstrated greater than 33 dB gain over a 4 GHz bandwidth with a noise figure of less than 2 dB over 2 GHz. The Q-Band power amplifier has demonstrated an output power of 13.3 dBm at 1 dB compression with 25.3 dB of gain and a saturated output power of 16.1 dBm at 40 GHz. These amplifiers are designed for insertion into future EHF satellite communication ground terminals.

INTRODUCTION

Monolithic 20 GHz low noise amplifiers (LNA) and 44 GHz power amplifiers are important building blocks for future EHF SATCOM ground terminals, which strive for high reliability, small size and weight, and low power consumption [1]. previous work on the monolithic 20 GHz low noise amplifier [2] used AlGaAs/GaAs HEMT devices and a quasi-hybrid off-chip input matching network to achieve its low noise figure. This work reports a fully monolithic 20 GHz LNA with on-chip input matching network achieving performance comparable to hybrid or quasi-hybrid approaches. This data represents the best reported gain and noise figure for a 20 GHz MMIC low noise amplifier using InGaAs HEMT devices.

Though there are several low noise or small signal Q-Band MMIC amplifiers reported previously [3,4], there has been no reported power performance of a Q-Band MMIC amplifier. This work reports a an amplifier design suitable for use as the driver stage of a Q-Band transmitter. This work demonstrates that high performance LNAs and power amplifiers can be processed using a single psuedomorphic InGaAs HEMT technology. This feature is important for compact microwave and millimeter wave T/R module applications.

HEMT DEVICES AND MMIC PROCESS

The InGaAs psuedomorphic HEMT structure was chosen for its low noise characteristics while its power capabilities were of secondary concern. Figure 1 shows a cross section of InGaAs HEMT device. The AlGaAs/InGaAs heterojunction structure was grown by MBE technique. The AlGaAs region is planar-doped

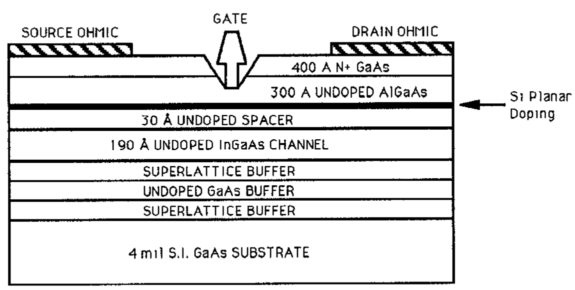

Figure 1. Psuedomorphic InGaAs HEMT Device Structure.

with Si for higher breakdown voltage and 22% indium concentration is employed in the channel for higher electron mobility and saturation velocity. The 0.2 micron T-shaped gate was patterned by a two-layer photoresist electron beam lithography process. The metal, dielectric, air-bridge, and backside levels of the MMIC process were all carried-out using photolithography techniques.

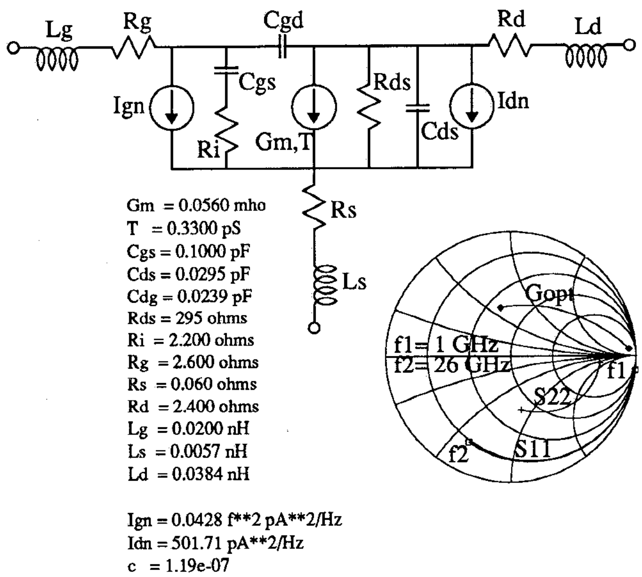

Figure 2. 120 Micron Low Noise HEMT Model

DEVICE NOISE MODELING AND LNA DESIGN

Figure 2 shows the device small signal model with element values and a Smith chart showing the modeled S11, S22, and optimum noise input match (Gopt) for a 120 micron HEMT device. The model includes the correlated noise source circuit element available in EESOF's LIBRA program. The noise parameters (Fmin, Gopt, Rn) and S-Parameters of the HEMT device were measured on-wafer using a noise measurement test set from ATN, Inc. The elements of the LIBRA FET model, with the added noise elements and parasitics, were optimized to achieve the best fit to the measured data.

This HEMT model was then used to design the matching networks for the 3-stage LNA. A schematic of the design is shown in Figure 3.

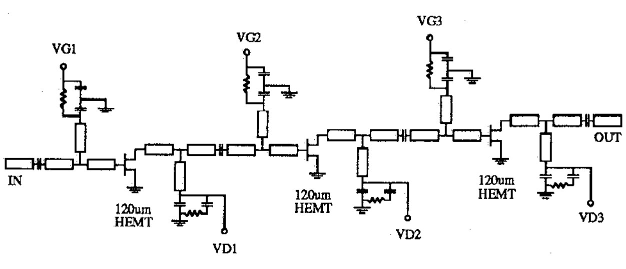

Figure 3. Schematic of 3-Stage MMIC LNA.

The design uses shorted stubs for the matching elements and on-chip bias networks consisting of thin-film resistors and MIM capacitors for bypass purposes. The bias is injected through the shorted stubs, where MIM capacitors are used as DC blocks.

The input matching network was designed to give the best possible noise figure while maintaining a good associated gain. High impedance inductive transmission lines were added between the source of the FETs and the ground vias to improve the input match and for increased stability. The second and third stage matching networks were designed to give the best gain while remaining unconditionally stable. A photo of the completed circuit is shown in Figure 4.

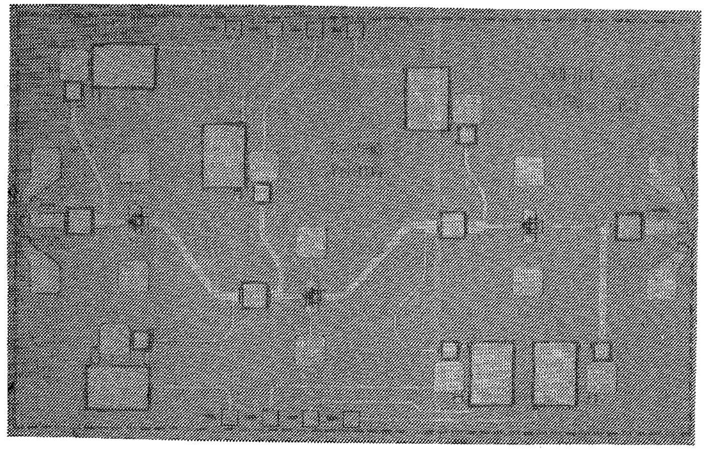

Figure 4. Completed 20 GHz MMIC LNA.

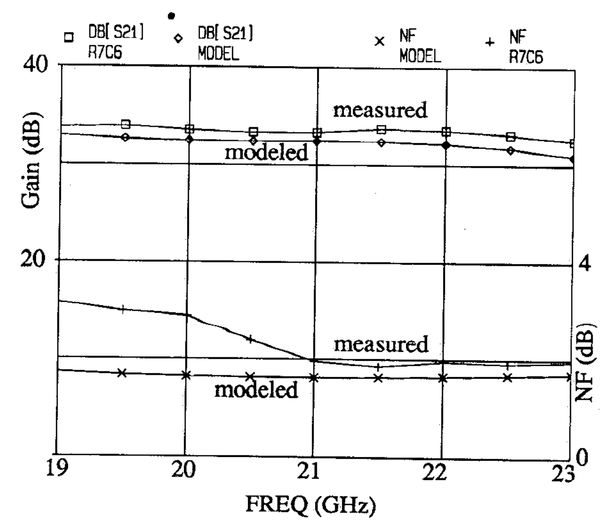

Figure 5. Measured and Modeled Gain and Noise Figure of InGaAs HEMT MMIC LNA.

LNA MEASUREMENT RESULTS

The 20 GHz LNA circuit was tested for noise figure and associated gain with the bias of the first stage adjusted to give best noise figure. The second and third stages are biased to give best gain. The measured gain and noise figure are shown in Figure 5 along with predicted performance, based on the HEMT model shown previously and the analysis performed with LIBRA. The gain is 33 dB or better across a 4 GHz bandwidth and the noise figure is below 2 dB from 21 GHz to 23 GHz. The LNA circuits were tested on-wafer using the ATN system, which allows for calibrated 50 ohm noise figure measurements.

Q-BAND POWER AMPLIFIER DESIGN

The Q-Band power amplifier utilizes 80 micron HEMT devices in the first two stages and a 150 micron device to provide added power output in the third stage. The amplifier was designed with small-signal models optimized

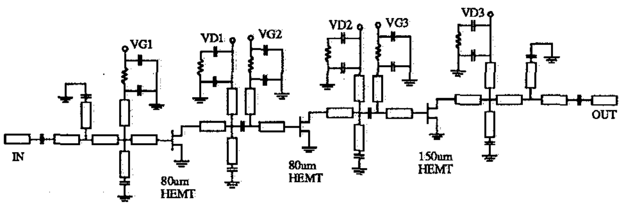

Figure 6. Schematic of Q-Band MMIC Power Amplifier.

from measured device S-parameter data. A schematic of the amplifier is shown in Figure 6. Shorted stubs are used in the matching networks and the gate and drain biases are injected through RF-shorted high-impedance quarter wavelength lines. DC blocking between stages and at the shorted stubs is provided by MIM capacitors. A photo of the completed chip is shown in Figure 7.

POWER AMPLIFIER MEASUREMENT RESULTS

The Q-Band amplifier was measured in a WR-22 waveguide test fixture with 5 mil quartz finline waveguide-to-microstrip transitions

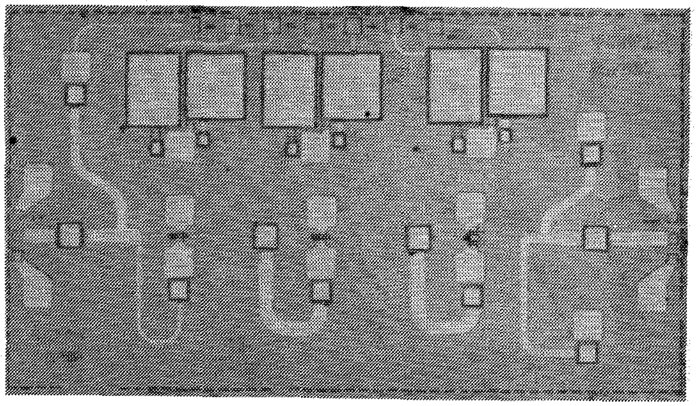

Figure 7. Completed Q-Band HEMT Amplifier.

shown in Figure 8. The data has been corrected for losses in the waveguide transitions. The small signal gain is shown in Figure 9 and is better than 25 dB from 35 to 40 GHz for an input power of -15 dBm. Figure 10 shows the power output of the amplifer as a function of the power in at 44.5 GHz. and Figure 11 shows the Pout vs Pin at 40 GHz. At 40 Ghz the 1 dB compression point gives 13.3 dBm of output power with 25.3 dB gain and the saturated output power is 16.1 dBm with 19.1 dB gain. The output power as a function of frequency is shown in Figure 12 for a fixed input power of -5 dBm.

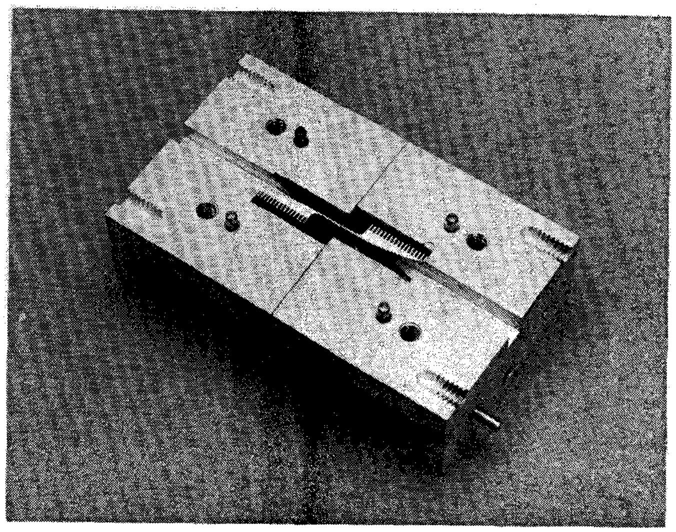

Figure 8. WR-22 Waveguide Test Housing

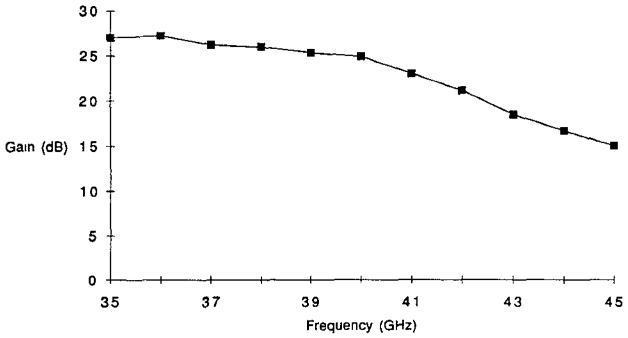

Figure 9. Gain of Q-Band Power Amplifier.

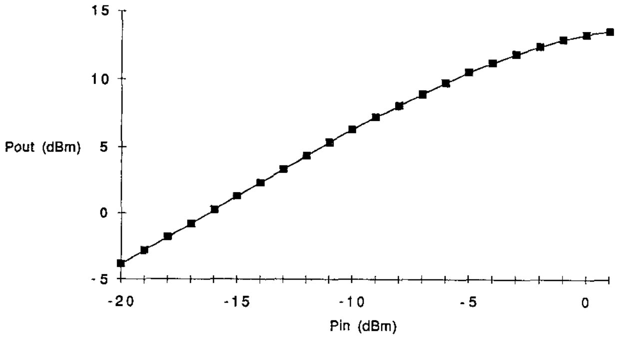

Figure 10. Pout vs. Pin of Amplifier at 44.5 GHz.

CONCLUSION

We have demonstrated superior performance in both low noise and power MMIC circuits utilizing the same InGaAs Pseudomorphic HEMT process. The 20 GHz LNA with gain of 33 dB and a noise figure of less than 2 dB can be used as the front end of a receiving system. The Q-Band power amplifer with 16.1 dBm saturated output power and 19.1 dB gain can be used as a driver amplifier in a transmitter application. Process compatibilty between the two circuits increases the potential for higher level integration and the attractive concept of an entire transceiver on a single MMIC chip.

ACKNOWLEDGEMENTS

This work is supported in part by the Air Force Rome Development Center, Griffiss AFB, NY under Contract No. F30602-89-C-0122. RADC program manager is William Cook. The authors wish to extend special thanks to Donald Tait and Diane Garske for their measurement expertise.

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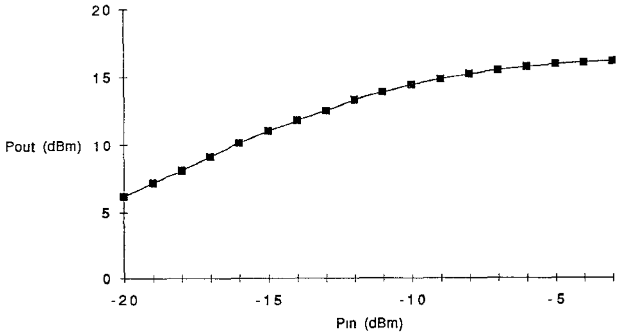

Figure 11. Output Power for MMIC HEMT Amplifier at 40 GHz.

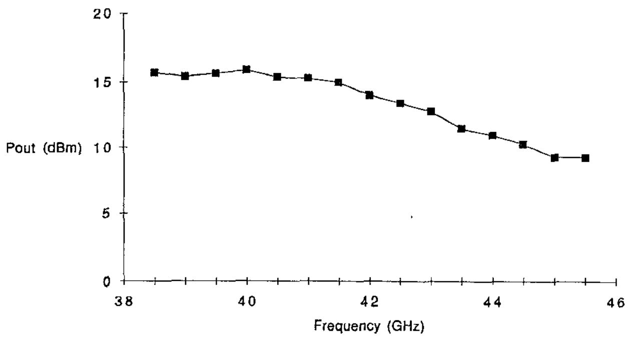

Figure 12. Output Power vs. Frequency for Amplifier at Pin = -5 dBm.